

SIP-HV1A05DS High Voltage Reed Relay Datasheet

MiRelay model-level engineering reference for RFQ, cross-reference review and preliminary design-in. Company: SHR AUTOSENSOR TECH LIMITED. Website: www.reed-relay.com. Email: sales@reed-relay.com. Phone/WhatsApp: +86 137 6157 1029.



Product image is representative. Marking, terminal details and accessories can vary by exact option and customer drawing.

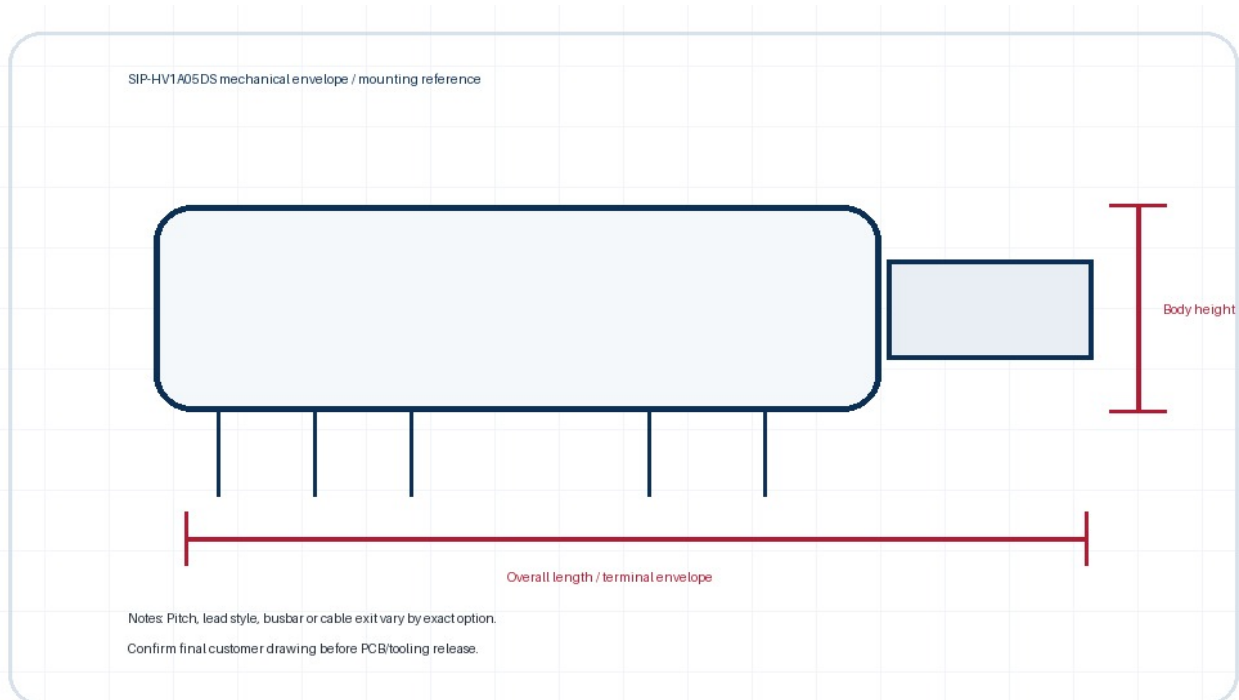
Key selection parameters

Parameter	Engineering note
Voltage class	4 kV to 20 kV family options
Contact form	1A / 1B / 1C / 2A and module variants
Coil voltage	5 / 12 / 24 VDC common options
Applications	Hipot, cable test, insulation monitoring, medical/industrial HV switching

Ordering code interpretation

Code block	Meaning
SIP-HV	SIP high-voltage reed relay family
1A	Normally-open contact form
05/12/24	Coil voltage option
D/S/LP	Diode, shield or low-profile option where specified

Mechanical envelope and drawing guidance



This drawing is an engineering envelope illustration prepared for selection and RFQ discussions. Use the final signed MiRelay drawing for PCB layout, mounting holes, busbar design, wire/cable exit, creepage/clearance and tooling release.

RFQ / design-in checklist

Breakdown and isolation margin
Load type: resistive, capacitive or pulse
Creepage/clearance and PCB layout
Coil suppression and drive circuit
Final drawing and safety validation

Required information for quotation

Please send target model or competitor part number, electrical ratings, load type, coil/control voltage, package limits, environmental requirements, sample quantity and annual forecast to sales@reed-relay.com. Attach drawings or PCB constraints when available.

Important notice

Preliminary engineering document. Specifications are derived from MiRelay family references and local product assets; they are not a substitute for final approval drawings, signed datasheets, customer validation or safety certification review. Mercury-wetted, high-voltage, medical, EV and PV applications require application-specific validation.